# 제21회 한국반도체학술대회

2014년 2월 24일(월)~26일(수) 한양대학교 서울캠퍼스, 서울

창조경제 실현을 위한 융합반도체

다가오는 2014년 갑오년(甲午年) 새해,
뜻 하신 바 모두 이루시길 기원합니다.

제21회 한국반도체학술대회 조직위원회 일동

## Advance Program 공지 안내

12월 27일 (금), 채택 논문 교신저자 및 발표자의 이메일로 논문 발표 일정 등 발송 되었습니다. 채택 논문의 발표에 대한 자세한 일정과 장소가 포함된 프로그램을 홈페이지에서 확인하실 수 있습니다. 참석자 및 논문 발표자께서는 발표 시간 및 발표장소를 미리 확인하시기 바랍니다

제21회 한국반도체학술대회 Advance Program 안내

The 21st Korean Conference on Semiconductors
제21회 한국반도체학술대회
February 24-26, 2014 / Hanyang University, Seoul, Korea

L. Analog Design 분과

## [TF1-L] 아날로그 및 혼성 신호 회로 설계 1

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|---|---|
| **Date** | Feb. 25, 2014 (Tue.) |
| **Place** | Room F / 제1공학관 404호 (# 404, Engineering Building I) |

Session Chair: 박성민 교수(이화여자대학교), 문용 교수(숭실대학교)

**TF1-L-1** **09:30-09:45**
**Area-Efficient 20-Gbps Optical Receiver Circuit in 65-nm CMOS Technology**
저자: Hyun-Yong Jung, Jin-Sung Youn, and Woo-Young Choi
소속: Department of Electrical and Electronic Engineering, Yonsei University

**TF1-L-2** **09:45-10:00**
**입력 지터 감소 기법을 적용한 2.5 Gb/s BMCDR 회로 설계**
저자: 정재훈[1], 최정환[1], 백광현[2]
소속: [1]삼성전자 메모리사업부, [2]중앙대학교 전자전기공학부

**TF1-L-3** **10:00-10:15**
**A Single-Stage 40dB-Linear Digitally-Controlled Variable Gain Amplifier for Ultrasound Analog Front End**
저자: Seong-Eun Cho[1], Ji-Yong Um[2], Byungsub Kim[2], Jae-Yoon Sim[2], and Hong-June Park[1,2]
소속: [1]Division of IT Convergence Engineering, Pohang University of Science and Technology, [2]Department of Electronic and Electrical Engineering, Pohang University of Science and Technology

**TF1-L-4** **10:15-10:30**
**Constant Off-Time Control with Time Calibration Method for Buck Converter**
저자: Haneul Kim, Kyoungjin Lee, Jehyung Yoon, Hyoung-Seok Oh, and Byeong-Ha Park
소속: Power Device Development Team, System LSI Division, Samsung Electronics Co., Ltd.

**TF1-L-5** **10:30-10:45**
**A 25-Gb/s Quarter-Rate CDR in 65-nm CMOS Technology**
저자: Dae-Hyun Kwon and Woo-Young Choi
소속: Department of Electrical and Electronic Engineering, Yonsei University

**TF1-L-6** **10:45-11:00**
**A Multi-Channel 1-Gb/s/ch Inverter Transimpedance Amplifier Array with Replica in 0.18μm CMOS**
저자: Hanbyul Choi, Xiao Ying, Seung-Hoon Kim, and Sung Min Park
소속: Department of Electronics Engineering, Ewha Womans University

# Area-Efficient 20-Gbps Optical Receiver Circuit in 65-nm CMOS Technology

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Recently, the demands for high-speed optical receivers with small chip-area are increasing for optical interconnect applications. The popular technique of circuit bandwidth enhancement with passive inductors require a large chip area and may not be suitable for certain applications with tight cost requirements [1-2]. We investigate the maximum receiver circuit bandwidth possible within standard 65-nm CMOS without using passive inductors. The receiver circuit is composed of transimpedance amplifier (TIA) with DC-balancing buffer, post amplifier (PA), and output buffer. The TIA is designed in the shunt-feedback configuration with active feedback. The PA is a 6-stage differential amplifier with interleaved active feedback. The measured transimpedance gain and 3-dB bandwidth of the fabricated optical receiver circuit are 74.5 dBΩ and 12 GHz, respectively. With the fabricated receiver circuit, 20-Gb/s $2^{31}-1$ electrical pseudo-random bit sequence data are successfully received with the bit-error rate less than $10^{-12}$. The receiver circuit has a small chip area of 0.13 mm × 0.3 mm. The power consumption excluding the output buffer is 120 mW with 1.2-V supply voltage.

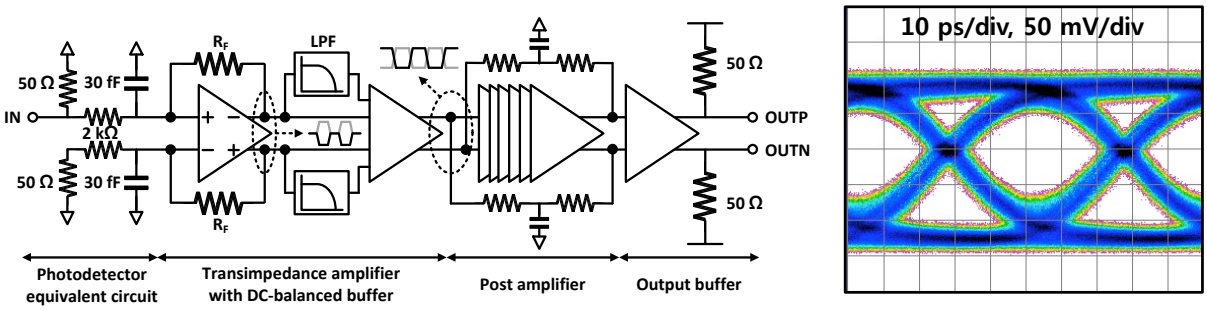


Fig 1. Block diagram and 20-Gbps eye diagram of the optical receiver circuit.

[1] C. Kromer, G. Sialm, T. Morf, M. L. Schmatz, F. Ellinger, D. Erni, and H. Jäckel, "A low-power 20-GHz 52-dBΩ transimpedance amplifier in 80-nm CMOS," J. Solid-State Circuits, vol. 39, no. 6, pp. 885-894 (2004).

[2] T. Takemoto, F. Yuki, H. Yamashita, Y. Lee, T. Saito, S. Tsuji, and S. Nishimura, "A compact 4 x 25-Gb/s 2.0 mW/Gb/s CMOS-based optical receiver for board-to-board interconnects," J. Lightwave Tech., vol. 28, pp. 3343-3350 (2010).